Amendments to the Specification

Please replace the paragraph beginning at page 7, line 15 with the following amended paragraph:

A method of driving a liquid crystal panel according to still another aspect of the present invention, as embodied herein, includes steps of: applying scanning signal voltages each having a width ~~enlarged~~ reduced in accordance with a position at the signal wire to the scanning wire; and supplying data signal voltages to the signal wire.

Please replace the paragraph beginning at page 7, line 21 with the following amended paragraph:

A method of driving a liquid crystal panel according to still another aspect of the present invention, as embodied herein, includes steps of: applying scanning signal voltages each having a width ~~enlarged~~ reduced in accordance with a position at the signal wire to the scanning wire; and supplying data signal voltages each having a width enlarged in accordance with a position at the scanning wire to the signal wire.

Please replace the paragraph beginning at page 9, line 3 with the following amended paragraph:

A driving apparatus for a liquid crystal panel according to still another aspect of the present invention, as embodied herein, includes: scanning side driving means for applying scanning signal voltages having a width ~~enlarged~~ reduced in accordance with a position of the signal wire to the scanning wire; and signal side driving means for supplying data signal voltages having a width enlarged in accordance with a position of the scanning wire to the signal wire.

Please replace the paragraph beginning at page 28, line 10 with the following amended paragraph:

Meanwhile, the second controller 42 responds to a vertical synchronous signal VS from first synchronous line 41, the horizontal synchronous signal HS from second synchronous line 43 and

the data clock DCLK from the clock line 37. The second controller 42 generates a gate output enable signal GOE, as shown in Fig. 19, on the basis of the data clock DCLK and the horizontal and vertical synchronous signals HS and VS, and applies the gate output enable signal GOE to the first to fifth gate driver IC chips 32A to 32E. The gate output enable signal GOE has an enable width (i.e., a low logic interval) which is gradually ~~increased~~ decreased every horizontal synchronous period by a predetermined interval, during one vertical synchronous period. The first and fifth gate driver IC chips 32A to 32E responding commonly to the gate output signal GOE from the second controller 42, generate m scanning signals GSS1 to GSSm having widths to be gradually ~~increased~~ decreased by a predetermined interval, as shown in Fig. 20. The m scanning signals GSS1 to GSSm are applied to the m gate lines GL1 to GLm such that signal charging period of each liquid crystal cell connected to one data line DL are gradually ~~elongated~~ reduced by the predetermined interval. In other words, the signal charging period of each liquid crystal cell appears as timing signals CSS1 to CSSm shown in Fig. 21. The predetermined width is set in such a manner that a data signal transferred over the data line corresponds to a time interval passing through a distance in which two gate lines are arranged. Accordingly, even when a data signal transferred from the start point of data line DL (i.e., the top portion) into the final point of data line DL (i.e., the bottom portion) is delayed, the data signals are accurately applied to the liquid crystal cells on the gate lines. Also, the charging time of each the liquid crystal cell on the liquid crystal panel becomes uniform. As a result, an accurate data signal is applied to each liquid crystal cell included in the liquid crystal panel 30, and hence a picture displayed on the liquid crystal panel 30 is not distorted.

Please replace the paragraph beginning at page 29, line 15 with the following amended paragraph:

Such a uniformity of the charging time in the liquid crystal cells will be identified through a simulation for a liquid crystal panel having 1024 data lines and 768 scanning lines. In the simulation, the 1024 data lines are grouped into 8 gate sub blocks GSB1 to GSB8 and the 768 scanning lines are grouped into 8 data sub blocks DSB1 to DSB8. In other words, the liquid crystal panel having 1024x768 picture elements (i.e., pixels) is divided into M sub blocks as

shown in Fig. 22. Each scanning signal GSS1 to GSS768 has a width ~~enlarged~~ reduced gradually in accordance with the gate sub blocks GSB1 to GSB8. In detail, the width of each the scanning signal GSS1 to GSS768 is gradually reduced from the width corresponding to the period of the horizontal synchronous signal HS in accordance with proceeding from the top gate sub block GSB1 to the bottom gate sub block GSB8, as seen in Figs. 23A and 23B. Then, the disable period (i.e., the high logic interval) of the gate output enable signal GOE is gradually enlarged in accordance with proceeding from the top gate sub block GSB1 to the bottom gate sub block GSB8, as seen in Figs. 23A and 23B. Similarly, the data signal DS has a different width according to the data sub blocks DSB1 to DSB8. In detail, the width of the data signal DS is gradually reduced from the width corresponding to the period of the horizontal synchronous signal HS in accordance with proceeding from the right side data sub block DSB8 to the left side data sub block DSB1, as seen in Figs. 24A and 24B. The data signal DS to be applied to the right side data sub block DSB8 have a width nearly equal to the width corresponding to the period of the horizontal synchronous signal HS. The disable period (i.e., the high logic interval) of the data output enable signal /DOE is gradually enlarged in accordance with proceeding from the right side data sub block DSB8 to the left side data sub block DSB1, as seen in Figs. 24A and 24B. Since the data and scanning signals DS and GSS are varied along with the sub blocks DSB1 to DSB8 and GSB1 to GSB8, the M sub blocks on the liquid crystal panel each receives a data signal DS1 to DS8 and a scanning signal GSS1 to GSS8, as shown Fig. 25.